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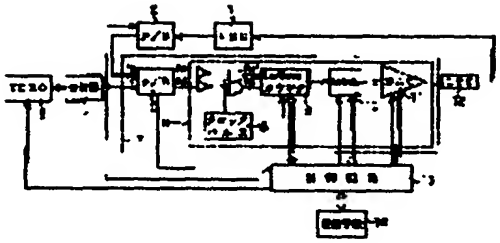
(54) PLL SYNTHESIZER

(57)Abstract:
PURPOSE: To provide the PLL synthesizer consisting of parts where charge pump control and storage are easy.
CONSTITUTION: A charge pump 6 consists of an up/down counter 9 which counts the phase difference between an up signal Pu and a down signal Pd of a phase comparator 5, a latch 10 where the output value of the up/down counter 9 is held, and a digital-analog converter 11 which converts the output of the latch 10 into an analog signal. Thus, power saving and temperature correction are facilitated, and the strength against noise is improved. For the purpose of shortening the lock-up time, it is unnecessary to prepare ana switch two charge pumps or to propare and switch two resistances.



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CLAIMS

[Claim(s)]

[Claim 1] A voltage controlled oscillator and the programmable divider which carries out dividing of the output of this voltage controlled oscillator in adjustable, The phase comparator which outputs the rise signal Pu which detects the phase contrast of the output from reference frequency VCO and this frequency VCO, and the output of a programmable divider, and shows this phase contrast by pulse width, and the down signal Pd, In the PLL synthesizer which consisted of low-pass filters which change into the control voltage to a voltage controlled oscillator the voltage of the charge pump which changes the rise signal Pu from this phase comparator, and the down signal Pd into voltage, and this charge pump The counter the aforementioned charge pump counts [counter] the phase contrast of the aforementioned rise signal Pu and the down signal Pd, The PLL synthesizer characterized by consisting of a latch holding the output value of this counter, and a digital analog converter which changes the output of this latch into an analog signal.

[Claim 2] The PLL synthesizer indicated to the claim 1 characterized by having the control circuit which controls change of the aforementioned control voltage based on a storage means to memorize the data concerning the output of the aforementioned counter, and this storage means.

[Claim 3] The PLL synthesizer indicated to the claim 1 characterized by having the control circuit which has by the output value of the aforementioned counter corresponding to the division ratio changed based on the aforementioned storage means, and controls the aforementioned latch when there are a storage means to memorize the correlation of the output value of the aforementioned counter and the division ratio of a programmable divider, and change of a division ratio.

[Claim 4] It is the PLL synthesizer indicated to the claim 1 characterized by having a control circuit and a storage means, outputting the output of the latch which the aforementioned control circuit made the aforementioned storage means memorize the output of a latch, and was memorized by the aforementioned storage means to a digital analog converter, and intercepting at least one between a voltage controlled oscillator and a digital analog converter.

[Claim 5] It is the PLL synthesizer indicate holding the output-control voltage of the aforementioned low-pass filter in front of power-saving operation to the claim 1 carry out as the feature by making the aforementioned programmable divider into non-actuation by having the control circuit to which power-saving operation is made to perform, and a storage means, and the aforementioned control circuit's making the aforementioned storage means memorize the output of the aforementioned counter in front of power-saving operation, and controlling the aforementioned latch based on the aforementioned storage means at the time of power-saving operation.

[Claim 6] The PLL synthesizer indicated to the claim 1 characterized by having the control circuit which has by the output value of the aforementioned counter in a predetermined division ratio based on a storage means to memorize the correlation of the temperature of the reference frequency VCO in which temperature compensation is possible, and the output value of the aforementioned counter in a predetermined division ratio and reference frequency VCO, and the aforementioned storage means, and carries out temperature compensation of the reference frequency VCO.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the PLL synthesizer which has a charge pump.
[0002]
[Description of the Prior Art] Many PLL synthesizers to radio, portable telephone, etc. are used. There is a charge pump which changes the phase contrast signal from a phase comparator into the voltage to a low-pass filter in this PLL synthesizer. This charge pump consists of two FET (Field Effect Transisitor) so that it may be indicated by JP,58-22343,Y. Operation of a charge pump is explained. Drawing 5 is a block diagram of a PLL synthesizer which has a charge pump (15) as shown in drawing 6 , and drawing 7 is a timing chart which shows operation of a phase comparator (phi/D) (5) and a charge pump (15). fp of these drawings is the output from a voltage controlled oscillator by which dividing was carried out by the programmable divider, and fr is the output from reference frequency VCO by which dividing was carried out with the counting-down circuit. If fp and fr are inputted into a phase comparator, only while the phase of fp is progressing rather than fr, the rise signal Pu of a phase comparator serves as Low, and while the phase of fp is behind fr, the down signal Pd of a phase comparator serves as Low. If each of fp(s) and fr(s) is High(s), each FET of both of a charge pump is in an OFF state, and the capacitor of a low-pass filter (12) holds fixed potential, and holds a lock. However, when Pu is set to Low, the capacitor of a low-pass filter (12) is made to charge, and when Pd is set to Low, the capacitor of a low-pass filter is made to discharge. In this way, the always stabilized oscillation frequency can be obtained from a voltage controlled oscillator.
[0003]
[Problem(s) to be Solved by the Invention] Since the conventional charge pump consisted of FET of the above analogs, it was not easy to control by the control circuit or to memorize the value of a charge pump. For this reason, based on the value of a charge pump, control of PLL operation, such as power saving and temperature compensation, was difficult. Moreover, since control of a charge pump was difficult, the conventional PLL control had the problem of taking lock-up time for a long time, when a change of a division ratio was made greatly, in order to start feedback control from the state at that time, when a change of a division ratio is made.
[0004] Furthermore, since the charge pump of the conventional example had amended the control voltage of a low-pass filter by charge and electric discharge like ****, the time constant of a low-pass filter (12) needed to be changed to shortening lock-up time. For this reason, as shown in drawing 8 , a charge pump (15) and two (16) were prepared, this needed to be changed by the CONT signal, and two resistance needed to be prepared and this needed to be changed with a switch (17).
[0005]
[Means for Solving the Problem] this invention was made in view of this point, and the 1st feature is that a charge pump consists of a counter which counts the phase contrast of the aforementioned rise signal Pu and the down signal Pd, a latch holding the output value of this counter, and a digital analog converter which changes the output of this latch into an analog signal.
[0006] The 2nd feature is having had the control circuit which controls change of the aforementioned control voltage based on a storage means memorizing the data concerning the output of the aforementioned counter, and this storage means.
[0007] The 3rd feature is having the control circuit which has by the output value of the aforementioned counter corresponding to the division ratio changed based on the aforementioned storage means, and controls the aforementioned latch, when a storage means to memorize the correlation of the output value of the aforementioned counter and the division ratio of a programmable divider, and change of a division ratio are.
[0008] It is the 4th feature's being equipped with a storage means, outputting the output of the latch which the aforementioned control circuit's made the aforementioned storage means memorize the output of a latch, and was memorized by the aforementioned storage means to a digital analog converter, and intercepting at least one between a voltage controlled oscillator and a digital analog converter.

[0009] It is holding the output-control voltage of the aforementioned low-pass filter in front of power-saving operation by equipping the 5th feature with the control circuit to which power-saving operation is made to perform by making a programmable divider into non-actuation, and a storage means, and the aforementioned control circuit's making the aforementioned storage means memorize the output of the aforementioned counter in front of power-saving operation, and controlling the aforementioned latch based on the aforementioned storage means at the time of power-saving operation.
[0010] The 6th feature is having the control circuit which has by the output value of the aforementioned counter in a predetermined division ratio based on a storage means memorizing the correlation of the temperature of the reference frequency VCO in which temperature compensation's is possible, and the output value of the aforementioned counter in a predetermined division ratio and reference frequency VCO, and the aforementioned storage means, and carries out temperature compensation of the reference frequency VCO.
[0011]
[Function] Storage of control or an output is easy and can constitute a charge pump. Thereby, temperature compensation of power saving which makes a programmable divider non-actuation, shortening of lock-up time, and the reference frequency VCO is carried out.
[0012]
[Example] The example of this invention is explained based on drawing. Drawing 1 is the block diagram of a PLL synthesizer. (1) is a voltage controlled oscillator (VCO) and it outputs desired frequency outside. (2) is a programmable divider (P/D) and it carries out dividing of the output of a voltage controlled oscillator (1) in adjustable. (3) is a temperature compensated crystal oscillator (TCXO), and it can tune oscillation frequency finely. (4) is a counting-down circuit and it carries out dividing of the output of a temperature compensated crystal oscillator (3). (5) is a phase comparator (phi/D) and it outputs the phase contrast of the output fr of a temperature compensated crystal oscillator (3) by which dividing was carried out to the output fp of a voltage controlled oscillator (1) by which dividing was carried out, and detection of a lock. Phase contrast is outputted by the rise signal Pu and the down signal Pd. (6) is a charge pump and it changes the rise signal Pu from a phase comparator (5), and the down signal Pd into voltage. A charge pump (6) is aligned with a phase comparator (5), and it is called the phase comparator (7) of a wide sense. On the other hand, (5) which does not contain a charge pump (6) is a phase comparator in a narrow sense. Here, a phase comparator in a narrow sense is only called phase comparator.
[0013] A charge pump (6) consists of a clock pulse (8), an updown counter (Up/Down counter) (9), and a latch (Latch) (10) and a digital analog converter (11) (DAC). An updown counter (9) counts each phase contrast from the rise signal Pu from a phase comparator (5), and the down signal Pd. A clock pulse (8) sends out the reference pulse signal for the count of an updown counter (9). A latch (10) holds the output of an updown counter (9). That is, the output of an updown counter (9) is temporarily memorizable. A digital analog converter (11) changes into the voltage according to counted value the output of the latch (10) which is a digital signal. (12) is a low-pass filter (LPF) and amends the control voltage to a voltage controlled oscillator (1) based on the output voltage of a digital analog converter (11).
[0014] (13) is a control circuit and controls each part. (14) is storage meanses, such as RAM and ROM, and memorizes data required for operation of a control circuit (13). For example, the correlation of the division ratio to the output of an updown counter (9) or temperature is memorized.
[0015] 12 is a timing chart which shows operation of a phase comparator (5) and an updown counter (9). If the output fp of a programmable divider (2) and the output fr of a counting-down circuit (4) are inputted into a phase comparator (5), only while the phase of fp is progressing rather than fr, the rise signal Pu of a phase comparator (5) serves as Low, and while the phase of fp is behind fr, the down signal Pd of a phase comparator (5) serves as Low. The pulse width of Low of Pu and Pd shows the phase contrast of fp and fr. This pulse width is changed into the signal (Pu' and Pd') expressed with the pulse width of High by the clock pulse (8) and the logical element (an inverter and AND gate). An updown counter (9) counts the pulse number of this Pu' and Pd', and outputs the value as a DESHITARU signal. The digital-output signal of an updown counter (9) is held by latch (10), and is changed into the voltage (analog) according to counted value (phase contrast) by the digital analog converter (11). The control voltage of a low-pass filter (12) is amended on this voltage.
[0016] Thus, if the phase of fp is progressing rather than fr, while the control voltage of a low-pass filter (12) was raised and the phase of fp is behind fr, the control voltage of a low-pass filter (12) is dropped. In this way, the always stabilized oscillation frequency can be obtained from a voltage controlled oscillator.
[0017] The above is the basic composition and basic operation of this invention, and has the following features.
[0018] ** Since the charge pump of the conventional example had amended the control voltage of a low-pass filter (12) by charge and electric discharge, it needed to change the time constant of a low-pass filter (12) to shortening lock-up time. For this reason, as shown in drawing 8 , two charge pumps were formed, this needed to be changed, and two resistance needed to be prepared and this needed to be changed. However, since the charge pump of this invention generates direct voltage, and in order for the speedup / speed down of applied voltage to a voltage controlled oscillator (1) to be dependent on the speed of a clock pulse (8), it is not necessary to take into consideration the time constant of a low-pass filter (12), and it has

neither a charge pump nor resistance doubly like before, or operation which changes this is not needed.
[0019] ** Since the processing inside a charge pump (6) is a digital signal, the digital control which used a microcomputer, RAM, the logical element, etc. is easy.
[0020] ** When a change of a division ratio is made, in order to start feedback control from the state at that time, the conventional PLL control takes lock-up time for a long time, when a change of a division ratio is made greatly. The control circuit (13) of this invention reads the correlation of a division ratio and the output value of an updown counter (9) from a storage means (14), when a setting change of a division ratio is made in a key stroke etc. (Y of S1), as shown in drawing 3 (S2). The tabular format of the updown counter (9) output value corresponding to the division ratio of it that is sufficient as a correlation, and the function by statistics, such as the least square method, is sufficient as it. By this correlation, the change value of the updown counter (9) corresponding to the change value of a division ratio is calculated, and this value is outputted to an updown counter (9) (S3). Feedback operation of PLL is performed by making this value into initial value (S4).
[0021] Furthermore, it has with the lock-up signal from a phase comparator (5) by the output value of (Y of S5), and the updown counter at this time (9), and the data of the aforementioned correlation of a storage means (14) are updated (S6).
(study)
[0022] Unless it carried out operation by the loop conventionally, the convergence value of attenuation was not found. However, since an updown counter (9) and a latch (10) are digital signals, this invention can output the voltage assumed easily from a charge pump (6). For this reason, lock-up time can be shortened and especially the effect when a change of a division ratio is made greatly is greatest.
[0023] ** Since an output is digital, a clock pulse (8) and a latch (10) are easy for a control circuit (13) to input into the next circuit the output value which made the storage means (14) memorize this output value, and made it memorize. And even if it intercepts between a voltage controlled oscillator (1) and a charge pump (6), the control voltage of a low-pass filter (12) can be held.
[0024] For example, as shown in drawing 4 , if the lock signal from a phase comparator (5) is received (S7), a control circuit (13) will make a storage means (14) memorize the output value of a latch (10) (S8), will read this output value from a storage means (14), and will output it to a digital analog converter (11) (S9). And between a latch (10) and digital analog converters (11) is intercepted (S10), and between a phase comparator (5) and charge pumps (6) is intercepted (S11). Next, supply (not shown) of the power supply to a programmable divider (2) is intercepted, and this is made into non-actuation (S12).
[0025] Thus, although a loop is intercepted and a programmable divider (2) serves as non-actuation, the control voltage of a low-pass filter (12) can be held by the output value of the latch (10) memorized. And by intercepting a loop, even if the noise by change of a phase comparator (5) is lost and a noise arises, a noise cannot carry out a loop and a PLL synthesizer strong against a noise can be supplied. Furthermore, power consumption can be lessened by making a programmable divider (2) into non-actuation.
[0026] an above-mentioned example -- especially -- power consumption -- although the large programmable divider (2) was made into non-actuation, even if it makes a counting-down circuit (4), a phase comparator (5), and an updown counter (9) into non-actuation, the output-control voltage of a low-pass filter can be held
[0027] Moreover, although DAC (11) was controlled by the above-mentioned example based on the output value of a latch (10), based on the output value of an updown counter (9), you may control a latch (10) (9).
[0028] ** Carry out small change of the frequency outputted from reference frequency VCO with temperature. For this reason, the control circuit (13) makes the storage means (14) memorize the correlation of the output value of an updown counter, and the temperature of reference frequency VCO in a predetermined division ratio beforehand. And temperature compensation of the reference frequency VCO is carried out to the division ratio set up from the output value of an updown counter using the correlation read from the storage means (14). Thereby, a temperature control with a high precision becomes possible.
[0029]
[Effect of the Invention] Since the processing inside a charge pump (6) is a digital signal, the digital control which used a microcomputer, RAM, the logical element, etc. is easy. This storage and control can perform power saving and temperature compensation. Moreover, a PLL synthesizer strong against a noise can be supplied.
[0030] Furthermore, in order to shorten lock-up time, two charge pumps are formed and the cure which changes this, or prepares two resistance and changes this is not needed.

[Translation done.]

TECHNICAL FIELD

[Industrial Application] this invention relates to the PLL synthesizer which has a charge pump.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Many PLL synthesizers to radio, portable telephone, etc. are used. There is a charge pump which changes the phase contrast signal from a phase comparator into the voltage to a low-pass filter in this PLL synthesizer. This charge pump consists of two FET (Field Effect Transisitor) so that it may be indicated by JP,58-22343,Y. Operation of a charge pump is explained. Drawing 5 is a block diagram of a PLL synthesizer which has a charge pump (15) as shown in drawing 6 , and drawing 7 is a timing chart which shows operation of a phase comparator (phi/D) (5) and a charge pump (15). fp of these drawings is the output from a voltage controlled oscillator by which dividing was carried out by the programmable divider, and fr is the output from reference frequency VCO by which dividing was carried out with the counting-down circuit. If fp and fr are inputted into a phase comparator, only while the phase of fp is progressing rather than fr, the rise signal Pu of a phase comparator serves as Low, and while the phase of fp is behind fr, the down signal Pd of a phase comparator serves as Low. If each of fp(s) and fr(s) is High(s), each FET of both of a charge pump is in an OFF state, and the capacitor of a low-pass filter (12) holds fixed potential, and holds a lock. However, when Pu is set to Low, the capacitor of a low-pass filter (12) is made to charge, and when Pd is set to Low, the capacitor of a low-pass filter is made to discharge. In this way, the always stabilized oscillation frequency can be obtained from a voltage controlled oscillator.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] Since the processing inside a charge pump (6) is a digital signal, the digital control which used a microcomputer, RAM, the logical element, etc. is easy. This storage and control can perform power saving and temperature compensation. Moreover, a PLL synthesizer strong against a noise can be supplied.
[0030] Furthermore, in order to shorten lock-up time, two charge pumps are formed and the cure which changes this, or prepares two resistance and changes this is not needed.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Since the conventional charge pump consisted of FET of the above analogs, it was not easy to control by the control circuit or to memorize the value of a charge pump. For this reason, based on the value of a charge pump, control of PLL operation, such as power saving and temperature compensation, was difficult. Moreover, since control of a charge pump was difficult, the conventional PLL control had the problem of taking lock-up time for a long time, when a change of a division ratio was made greatly, in order to start feedback control from the state at that time, when a change of a division ratio is made.

[0004] Furthermore, since the charge pump of the conventional example had amended the control voltage of a low-pass filter by charge and electric discharge like ****, the time constant of a low-pass filter (12) needed to be changed to shortening lock-up time. For this reason, as shown in drawing 8 , a charge pump (15) and two (16) were prepared, this needed to be changed by the CONT signal, and two resistance needed to be prepared and this needed to be changed with a switch (17).

[Translation done.]

MEANS

[Means for Solving the Problem] this invention was made in view of this point, and the 1st feature is that a charge pump consists of a counter which counts the phase contrast of the aforementioned rise signal Pu and the down signal Pd, a latch holding the output value of this counter, and a digital analog converter which changes the output of this latch into an analog signal.

[0006] The 2nd feature is having had the control circuit which controls change of the aforementioned control voltage based on a storage means memorizing the data concerning the output of the aforementioned counter, and this storage means.

[0007] The 3rd feature is having the control circuit which has by the output value of the aforementioned counter corresponding to the division ratio changed based on the aforementioned storage means, and controls the aforementioned latch, when a storage means to memorize the correlation of the output value of the aforementioned counter and the division ratio of a programmable divider, and change of a division ratio are.

[0008] It is the 4th feature's being equipped with a storage means, outputting the output of the latch which the aforementioned control circuit's made the aforementioned storage means memorize the output of a latch, and was memorized by the aforementioned storage means to a digital analog converter, and intercepting at least one between a voltage controlled oscillator and a digital analog converter.

[0009] It is holding the output-control voltage of the aforementioned low-pass filter in front of power-saving operation by equipping the 5th feature with the control circuit to which power-saving operation is made to perform by making a programmable divider into non-actuation, and a storage means, and the aforementioned control circuit's making the aforementioned storage means memorize the output of the aforementioned counter in front of power-saving operation, and controlling the aforementioned latch based on the aforementioned storage means at the time of power-saving operation.

[0010] The 6th feature is having the control circuit which has by the output value of the aforementioned counter in a predetermined division ratio based on a storage means memorizing the correlation of the temperature of the reference frequency VCO in which temperature compensation's is possible, and the output value of the aforementioned counter in a predetermined division ratio and reference frequency VCO, and the aforementioned storage means, and carries out temperature compensation of the reference frequency VCO.

[Translation done.]

OPERATION

[Function] Storage of control or an output is easy and can constitute a charge pump. Thereby, temperature compensation of power saving which makes a programmable divider non-actuation, shortening of lock-up time, and the reference frequency VCO is carried out.

[Translation done.]

EXAMPLE

[Example] The example of this invention is explained based on drawing. Drawing 1 is the block diagram of a PLL synthesizer. (1) is a voltage controlled oscillator (VCO) and it outputs desired frequency outside. (2) is a programmable divider (P/D) and it carries out dividing of the output of a voltage controlled oscillator (1) in adjustable. (3) is a temperature compensated crystal oscillator (TCXO), and it can tune oscillation frequency finely. (4) is a counting-down circuit and it carries out dividing of the output of a temperature compensated crystal oscillator (3). (5) is a phase comparator (phi/D) and it outputs the phase contrast of the output fr of a temperature compensated crystal oscillator (3) by which dividing was carried out to the output fp of a voltage controlled oscillator (1) by which dividing was carried out, and detection of a lock. Phase contrast is outputted by the rise signal Pu and the down signal Pd. (6) is a charge pump and it changes the rise signal Pu from a phase comparator (5), and the down signal Pd into voltage. A charge pump (6) is aligned with a phase comparator (5), and it is called the phase comparator (7) of a wide sense. On the other hand, (5) which does not contain a charge pump (6) is a phase comparator in a narrow sense. Here, a phase comparator in a narrow sense is only called phase comparator.

[0013] A charge pump (6) consists of a clock pulse (8), an updown counter (Up/Down counter) (9), and a latch (Latch) (10) and a digital analog converter (11) (DAC). An updown counter (9) counts each phase contrast from the rise signal Pu from a phase comparator (5), and the down signal Pd. A clock pulse (8) sends out the reference pulse signal for the count of an updown counter (9). A latch (10) holds the output of an updown counter (9). That is, the output of an updown counter (9) is temporarily memorizable. A digital analog converter (11) changes into the voltage according to counted value the output of the latch (10) which is a digital signal. (12) is a low-pass filter (LPF) and amends the control voltage to a voltage controlled oscillator (1) based on the output voltage of a digital analog converter (11).

[0014] (13) is a control circuit and controls each part. (14) is storage meanses, such as RAM and ROM, and memorizes data required for operation of a control circuit (13). For example, the correlation of the division ratio to the output of an updown counter (9) or temperature is memorized.

[0015] 12 is a timing chart which shows operation of a phase comparator (5) and an updown counter (9). If the output fp of a programmable divider (2) and the output fr of a counting-down circuit (4) are inputted into a phase comparator (5), only while the phase of fp is progressing rather than fr, the rise signal Pu of a phase comparator (5) serves as Low, and while the phase of fp is behind fr, the down signal Pd of a phase comparator (5) serves as Low. The pulse width of Low of Pu and Pd shows the phase contrast of fp and fr. This pulse width is changed into the signal (Pu' and Pd') expressed with the pulse width of High by the clock pulse (8) and the logical element (an inverter and AND gate). An updown counter (9) counts the pulse number of this Pu' and Pd', and outputs the value as a DESHITARU signal. The digital-output signal of an updown counter (9) is held by latch (10), and is changed into the voltage (analog) according to counted value (phase contrast) by the digital analog converter (11). The control voltage of a low-pass filter (12) is amended on this voltage.

[0016] Thus, if the phase of fp is progressing rather than fr, while the control voltage of a low-pass filter (12) was raised and the phase of fp is behind fr, the control voltage of a low-pass filter (12) is dropped. In this way, the always stabilized oscillation frequency can be obtained from a voltage controlled oscillator.

[0017] The above is the basic composition and basic operation of this invention, and has the following features.

[0018] ** Since the charge pump of the conventional example had amended the control voltage of a low-pass filter (12) by charge and electric discharge, it needed to change the time constant of a low-pass filter (12) to shortening lock-up time. For this reason, as shown in drawing 8 , two charge pumps were formed, this needed to be changed, and two resistance needed to be prepared and this needed to be changed. However, since the charge pump of this invention generates direct voltage, and in order for the speedup / speed down of applied voltage to a voltage controlled oscillator (1) to be dependent on the speed of a clock pulse (8), it is not necessary to take into consideration the time constant of a low-pass filter (12), and it has neither a charge pump nor resistance doubly like before, or operation which changes this is not needed.

[0019] ** Since the processing inside a charge pump (6) is a digital signal, the digital control which used a microcomputer, RAM, the logical element, etc. is easy.

[0020] ** When a change of a division ratio is made, in order to start feedback control from the state at that time, the conventional PLL control takes lock-up time for a long time, when a change of a division ratio is made greatly. The control circuit (13) of this invention reads the correlation of a division ratio and the output value of an updown counter (9) from a storage means (14), when a setting change of a division ratio is made in a key stroke etc. (Y of S1), as shown in drawing 3 (S2). The tabular format of the updown counter (9) output value corresponding to the division ratio of it that is sufficient as a correlation, and the function by statistics, such as the least square method, is sufficient as it. By this correlation, the change value of the updown counter (9) corresponding to the change value of a division ratio is calculated, and this value is outputted to an updown counter (9) (S3). Feedback operation of PLL is performed by making this value into initial value (S4).
[0021] Furthermore, it has with the lock-up signal from a phase comparator (5) by the output value of (Y of S5), and the updown counter at this time (9), and the data of the aforementioned correlation of a storage means (14) are updated (S6). (study)
[0022] Unless it carried out operation by the loop conventionally, the convergence value of attenuation was not found. However, since an updown counter (9) and a latch (10) are digital signals, this invention can output the voltage assumed easily from a charge pump (6). For this reason, lock-up time can be shortened and especially the effect when a change of a division ratio is made greatly is greatest.
[0023] ** Since an output is digital, a clock pulse (8) and a latch (10) are easy for a control circuit (13) to input into the next circuit the output value which made the storage means (14) memorize this output value, and made it memorize. And even if it intercepts between a voltage controlled oscillator (1) and a charge pump (6), the control voltage of a low-pass filter (12) can be held.
[0024] For example, as shown in drawing 4 , if the lock signal from a phase comparator (5) is received (S7), a control circuit (13) will make a storage means (14) memorize the output value of a latch (10) (S8), will read this output value from a storage means (14), and will output it to a digital analog converter (11) (S9). And between a latch (10) and digital analog converters (11) is intercepted (S10), and between a phase comparator (5) and charge pumps (6) is intercepted (S11). Next, supply (not shown) of the power supply to a programmable divider (2) is intercepted, and this is made into non-actuation (S12).
[0025] Thus, although a loop is intercepted and a programmable divider (2) serves as non-actuation, the control voltage of a low-pass filter (12) can be held by the output value of the latch (10) memorized. And by intercepting a loop, even if the noise by change of a phase comparator (5) is lost and a noise arises, a noise cannot carry out a loop and a PLL synthesizer strong against a noise can be supplied. Furthermore, power consumption can be lessened by making a programmable divider (2) into non-actuation.
[0026] an above-mentioned example -- especially -- power consumption -- although the large programmable divider (2) was made into non-actuation, even if it makes a counting-down circuit (4), a phase comparator (5), and an updown counter (9) into non-actuation, the output-control voltage of a low-pass filter can be held
[0027] Moreover, although DAC (11) was controlled by the above-mentioned example based on the output value of a latch (10), based on the output value of an updown counter (9), you may control a latch (10) (9).
[0028] ** Carry out small change of the frequency outputted from reference frequency VCO with temperature. For this reason, the control circuit (13) makes the storage means (14) memorize the correlation of the output value of an updown counter, and the temperature of reference frequency VCO in a predetermined division ratio beforehand. And temperature compensation of the reference frequency VCO is carried out to the division ratio set up from the output value of an updown counter using the correlation read from the storage means (14). Thereby, a temperature control with a high precision becomes possible.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the example of this invention.
[Drawing 2] It is the timing chart of an example.
[Drawing 3] The lock-up time of the control circuit of an example is drawing showing early operation.
[Drawing 4] It is drawing showing operation which serves as power saving in the noise of the control circuit of an example strongly.
[Drawing 5] It is the block diagram showing the composition of the PLL synthesizer which has the conventional charge pump.
[Drawing 6] It is drawing showing the composition of the conventional charge pump.
[Drawing 7] It is the conventional timing chart.
[Drawing 8] It is the block diagram which took the measures which bring the conventional lock-up time forward.
[Description of Notations]
1 Voltage Controlled Oscillator
2 Programmable Divider
3 Temperature Compensated Crystal Oscillator
4 Counting-down Circuit
5 Phase Comparator
6 Charge Pump
7 Phase Comparator
8 Clock Pulse
9 Updown Counter
10 Latch
11 Digital Signal Converter
12 Low-pass Filter
13 Control Circuit
14 Storage Means

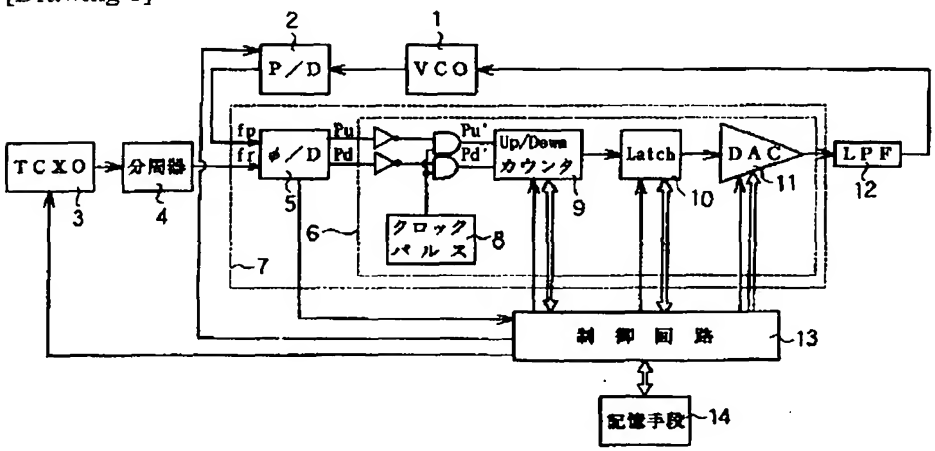
[Translation done.]

*'NOTICES *

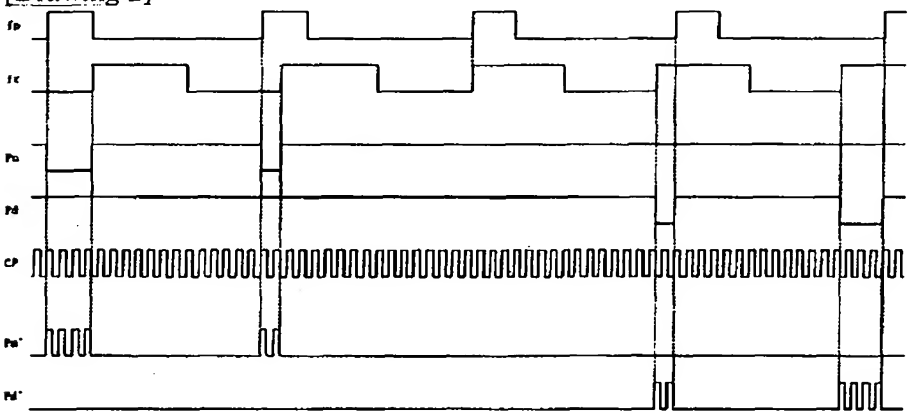
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

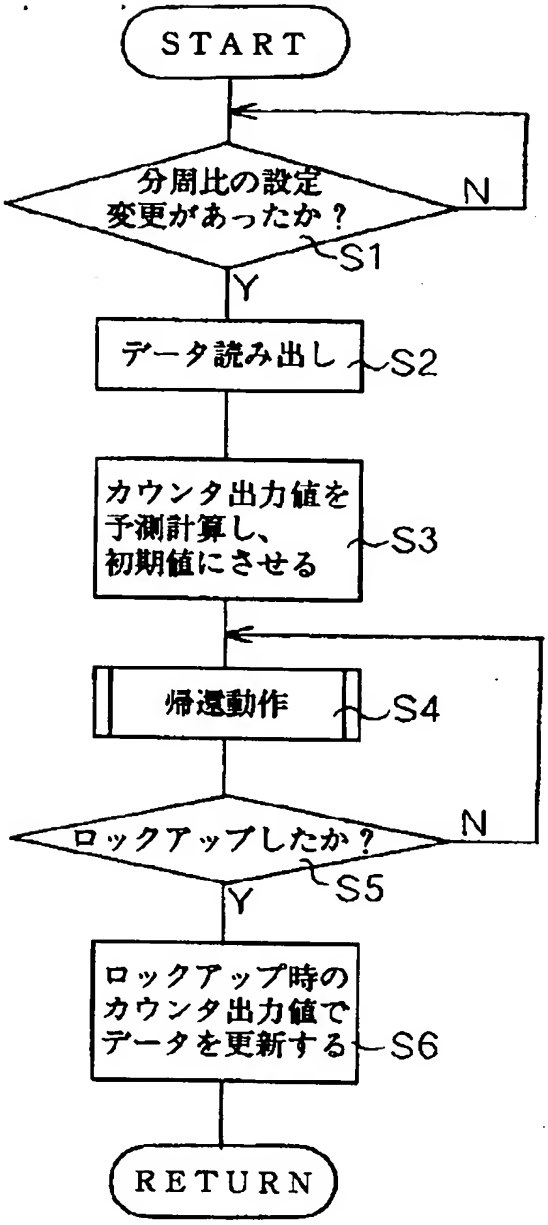
[Drawing 1]



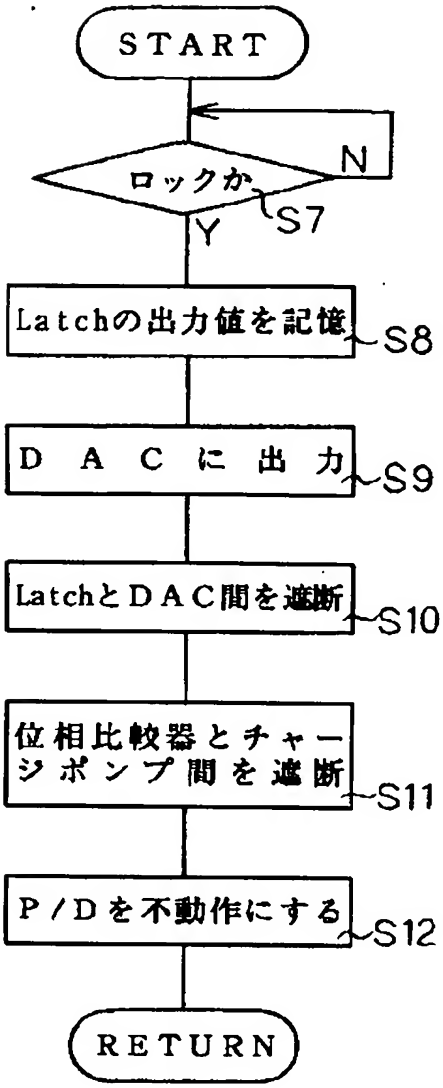
[Drawing 2]



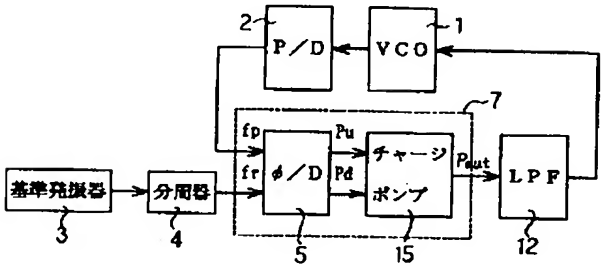
[Drawing 3]


START
分周比の設定
変更があったか？
N
S1
Y
データ読み出し
S2
カウンタ出力値を
予測計算し、
初期値にさせる
S3
帰還動作
S4
ロックアップしたか？
N
S5
Y
ロックアップ時の
カウンタ出力値で
データを更新する
S6
RETURN

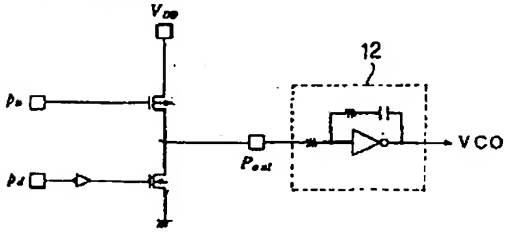
[Drawing 4]



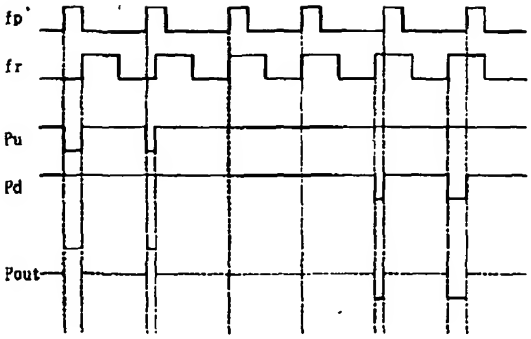
[Drawing 5]



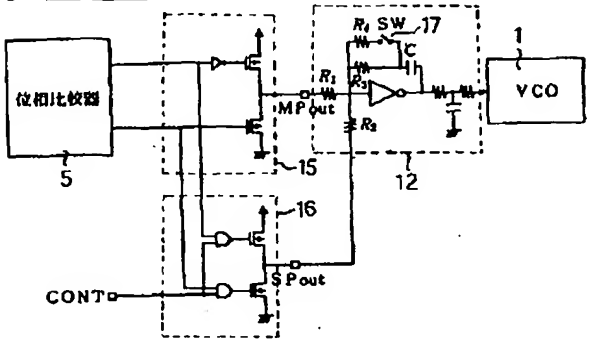
[Drawing 6]



[Drawing 7]



[Drawing 8]



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	7/093				7/08	Ｅ	
	7/089					Ｄ	

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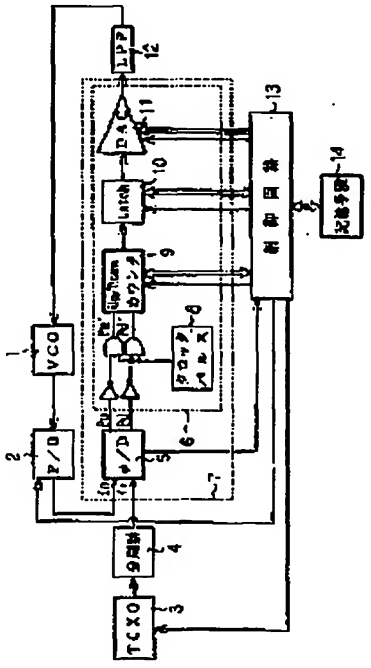
(54)【発明の名称】　ＰＬＬシンセサイザ

(57)【要約】
【目的】　チャージポンプの制御や記憶が容易な部品で構成されるＰＬＬシンセサイザーを供給する。
【構成】　チャージポンプ６を、位相比較器５のアップ信号Pu及びダウン信号Pdの位相差をカウントするアップダウンカウンタ９と、該アップダウンカウンタ９の出力値を保持するラッチ１０と、該ラッチ１０の出力をアナログ信号に変換するデジタルアナログコンバータ１１とで構成する。
【効果】　省電力や温度補正を容易に行うことができる。また、ノイズに強くすることができる。更に、ロックアップ時間を短縮するために、チャージポンプを２つ設けてこれを切り替えたり、抵抗を２つ設けてこれを切り替えたりする対策を必要としない。



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【特許請求の範囲】

【請求項１】　電圧制御発振器と、該電圧制御発振器の出力を可変的に分周するプログラマブル分周器と、基準周波数発振器と、該周波数発振器からの出力とプログラマブル分周器の出力の位相差を検出し該位相差をパルス幅で示すアップ信号Puおよびダウン信号Pdを出力する位相比較器と、該位相比較器からのアップ信号Puおよびダウン信号Pdを電圧に変換するチャージポンプと、該チャージポンプの電圧を電圧制御発振器への制御電圧に変換する低域濾波器で構成されたＰＬＬシンセサイザにおいて、前記チャージポンプが、前記アップ信号Puおよびダウン信号Pdの位相差をカウントするカウンタと、該カウンタの出力値を保持するラッチと、該ラッチの出力をアナログ信号に変換するデジタルアナログコンバータとで構成されることを特徴とするＰＬＬシンセサイザ。

【請求項２】　前記カウンタの出力に係るデータを記憶する記憶手段と、該記憶手段に基づき前記制御電圧の変動を制御する制御回路を備えたことを特徴とする請求項１に記載するＰＬＬシンセサイザ。

【請求項３】　前記カウンタの出力値とプログラマブル分周器の分周比の相関関係を記憶する記憶手段と、分周比の変更があるとき、前記記憶手段に基づき変更する分周比に対応する前記カウンタの出力値でもって前記ラッチを制御する制御回路を備えることを特徴とする請求項１に記載するＰＬＬシンセサイザ。

【請求項４】　制御回路と記憶手段とを備え、前記制御回路は、ラッチの出力を前記記憶手段に記憶させ、前記記憶手段に記憶されたラッチの出力をデジタルアナログコンバータに出力し、電圧制御発振器とデジタルアナログコンバータ間の少なくとも１箇所を遮断することを特徴とする請求項１に記載するＰＬＬシンセサイザ。

【請求項５】　前記プログラマブル分周器を不動作にさせることにより省電力動作を行わせる制御回路と、記憶手段とを備え、前記制御回路は、省電力動作直前の前記カウンタの出力を前記記憶手段に記憶させ、省電力動作時に前記記憶手段に基づき前記ラッチを制御することにより、省電力動作直前の前記低域濾波器の出力制御電圧を保持することを特徴とする請求項１に記載するＰＬＬシンセサイザ。

【請求項６】　温度補正可能な基準周波数発振器と、所定の分周比における前記カウンタの出力値と基準周波数発振器の温度の相関関係を記憶する記憶手段と、前記記憶手段に基づき所定の分周比における前記カウンタの出力値でもって基準周波数発振器を温度補正する制御回路を備えることを特徴とする請求項１に記載するＰＬＬシンセサイザ。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明はチャージポンプを有するＰＬＬシンセサイザに関する。

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【０００２】

【従来の技術】ＰＬＬシンセサイザはラジオや携帯用電話機等に多く使用されている。このＰＬＬシンセサイザには位相比較器からの位相差信号を低域濾波器への電圧に変換するチャージポンプがある。このチャージポンプは例えば実公昭５８－２２３４３号公報に開示される如く、２つのＦＥＴ（Field Effect Transistor）で構成される。チャージポンプの動作について説明する。図５は図６に示す様なチャージポンプ（１５）を有するＰＬＬシンセサイザのブロック図であり、図７は位相比較器（φ／Ｄ）（５）とチャージポンプ（１５）の動作を示すタイミングチャートである。これらの図のfpはプログラマブル分周器で分周された電圧制御発振器からの出力であり、frは分周器で分周された基準周波数発振器からの出力である。fpおよびfrが位相比較器に入力されると、fpの位相がfrよりも進んでいる間だけ位相比較器のアップ信号PuがLowとなり、fpの位相がfrよりも遅れている間は位相比較器のダウン信号PdがLowとなる。fpとfrがいずれもHighであればチャージポンプの各ＦＥＴは共にオフ状態にあり、低域濾波器（１２）のコンデンサーは一定電位を保持し、ロックを保持する。しかし、PuがLowになると低域濾波器（１２）のコンデンサーを充電させ、PdがLowになると低域濾波器のコンデンサーを放電させる。かくして、電圧制御発振器からは常に安定した発振周波数を得ることができる。

【０００３】

【発明が解決しようとする課題】従来のチャージポンプは上述のようなアナログのＦＥＴで構成されているために、制御回路で制御したり、チャージポンプの値を記憶することが容易ではなかった。このために、チャージポンプの値に基づいて、省電力や温度補正等のＰＬＬ動作の制御が困難であった。また、チャージポンプの制御は困難であった為、従来のＰＬＬ制御は分周比の変更が行われた場合、そのときの状態から帰還制御を開始するために、分周比の変更が大きく行われた場合は、ロックアップ時間が長くかかるという問題があった。

【０００４】さらに、上述の如く従来例のチャージポンプは充電と放電により低域濾波器の制御電圧を補正していたために、ロックアップ時間を短縮するには低域濾波器（１２）の時定数を変化させる必要があった。このために、図８に示すようにチャージポンプ（１５）、（１６）を２つ設けてこれをＣＯＮＴ信号で切り替えたり、抵抗を２つ設けてこれをスイッチ（１７）で切り替える必要があった。

【０００５】

【課題を解決するための手段】本発明はかかる点に鑑みてなされたもので、その第１の特徴は、チャージポンプが、前記アップ信号Puおよびダウン信号Pdの位相差をカウントするカウンタと、該カウンタの出力値を保持するラッチと、該ラッチの出力をアナログ信号に変換するデジ

タルアナログコンバータとで構成されることである。

【０００６】第２の特徴は、前記カウンタの出力に係るデータを記憶する記憶手段と、該記憶手段に基づき前記制御電圧の変動を制御する制御回路を備えたことである。

【０００７】第３の特徴は前記カウンタの出力値とプログラマブル分周器の分周比の相関関係を記憶する記憶手段と、分周比の変更があるとき、前記記憶手段に基づき変更する分周比に対応する前記カウンタの出力値でもって前記ラッチを制御する制御回路を備えることである。

【０００８】第４の特徴は記憶手段とを備え、前記制御回路は、ラッチの出力を前記記憶手段に記憶させ、前記記憶手段に記憶されたラッチの出力をデジタルアナログコンバータに出力し、電圧制御発振器とデジタルアナログコンバータ間の少なくとも１箇所を遮断することである。

【０００９】第５の特徴はプログラマブル分周器を不動作にさせることにより省電力動作を行わせる制御回路と、記憶手段とを備え、前記制御回路は、省電力動作直前の前記カウンタの出力を前記記憶手段に記憶させ、省電力動作時に前記記憶手段に基づき前記ラッチを制御することにより、省電力動作直前の前記低域濾波器の出力制御電圧を保持することである。

【００１０】第６の特徴は温度補正可能な基準周波数発振器と、所定の分周比における前記カウンタの出力値と基準周波数発振器の温度の相関関係を記憶する記憶手段と、前記記憶手段に基づき所定の分周比における前記カウンタの出力値でもって基準周波数発振器を温度補正する制御回路を備えることである。

【００１１】

【作用】チャージポンプを制御や出力の記憶が容易なもので構成することができる。これにより、プログラマブル分周器を不動作にする省電力や、ロックアップ時間の短縮や、基準周波数発振器を温度補正させる。

【００１２】

【実施例】本発明の実施例を図に基づき説明する。図１はＰＬＬシンセサイザのブロック図である。（１）は電圧制御発振器（ＶＣＯ）であり、所望の周波数を外部に出力する。（２）はプログラマブル分周器（Ｐ／Ｄ）であり、電圧制御発振器（１）の出力を可変的に分周する。（３）は温度補償水晶発振器（ＴＣＸＯ）であり、発振周波数を微調整可能である。（４）は分周器であり、温度補償水晶発振器（３）の出力を分周する。（５）は位相比較器（φ／Ｄ）であり、分周された電圧制御発振器（１）の出力fpと分周された温度補償水晶発振器（３）の出力frの位相差及びロックの検出を出力する。位相差はアップ信号Puとダウン信号Pdで出力される。（６）はチャージポンプであり、位相比較器（５）からのアップ信号Pu及びダウン信号Pdを電圧に変換する。位相比較器（５）とチャージポンプ（６）を合わせて広義の位相比較器（７）という。これに対し、チャージポンプ（６）を含まない（５）は狭義の位相比較器である。ここでは、狭義の位相比較器を単に位相比較器という。

【００１３】チャージポンプ（６）はクロックパルス（８）、アップダウンカウンタ（Up/Downカウンタ）（９）、ラッチ（Latch）（１０）とデジタルアナログコンバータ（ＤＡＣ）（１１）より構成される。アップダウンカウンタ（９）は位相比較器（５）からのアップ信号Pu及びダウン信号Pdより各位相差をカウントする。クロックパルス（８）はアップダウンカウンタ（９）のカウントのための基準パルス信号を送出する。ラッチ（１０）はアップダウンカウンタ（９）の出力を保持する。即ち、アップダウンカウンタ（９）の出力を一時的に記憶することができる。デジタルアナログコンバータ（１１）はデジタル信号であるラッチ（１０）の出力をカウント値に応じた電圧に変更する。（１２）は低域濾波器（ＬＰＦ）であり、デジタルアナログコンバータ（１１）の出力電圧に基づいて電圧制御発振器（１）への制御電圧を補正する。

【００１４】（１３）は制御回路であり、各部を制御する。（１４）はＲＡＭやＲＯＭ等の記憶手段であり、制御回路（１３）の動作に必要なデータを記憶する。例えば、アップダウンカウンタ（９）の出力に対する分周比や温度の相関関係を記憶する。

【００１５】１２は位相比較器（５）とアップダウンカウンタ（９）の動作を示すタイミングチャートである。プログラマブル分周器（２）の出力fp及び分周器（４）の出力frが位相比較器（５）に入力されると、fpの位相がfrよりも進んでいる間だけ位相比較器（５）のアップ信号PuがLowとなり、fpの位相がfrよりも遅れている間は位相比較器（５）のダウン信号PdがLowとなる。PuとPdのLowのパルス幅はfpとfrの位相差を示している。このパルス幅をクロックパルス（８）と論理素子（インバータとＡＮＤゲート）によりHighのパルス幅で表す信号（Pu′及びPd′）に変換する。アップダウンカウンタ（９）はこのPu′及びPd′のパルス数をカウントしてその値をデジタル信号として出力する。アップダウンカウンタ（９）のデジタル出力信号はラッチ（１０）にて保持され、デジタルアナログコンバータ（１１）にてカウント値（位相差）に応じた電圧（アナログ）に変換される。この電圧にて低域濾波器（１２）の制御電圧が補正される。

【００１６】このようにして、fpの位相がfrよりも進んでおれば低域濾波器（１２）の制御電圧が上昇させられ、fpの位相がfrよりも遅れている間は低域濾波器（１２）の制御電圧が降下させられる。かくして、電圧制御発振器からは常に安定した発振周波数を得ることができる。

【００１７】以上が本発明の基本構成と基本動作であ

り．以下のような特徴を有する。

【００１８】①従来例のチャージポンプは充電と放電により低域濾波器（１２）の制御電圧を補正していたために．ロックアップ時間を短縮するには低域濾波器（１２）の時定数を変化させる必要があった。このために，図８に示すようにチャージポンプを２つ設けてこれを切り替えたり、抵抗を２つ設けてこれを切り替える必要があった。しかしながら、本発明のチャージポンプは直接電圧を発生するために、また、電圧制御発振器（１）に対する印加電圧のスピードアップ／スピードダウンはクロックパルス（８）の速度に依存するために低域濾波器（１２）の時定数を考慮する必要はなく、従来のようにチャージポンプや抵抗を２重にもったり、これを切り替える動作は必要としない。

【００１９】②チャージポンプ（６）内部での処理がデジタル信号であるために．マイクロコンピュータやＲＡＭや論理素子等を使用したデジタル制御が容易である。

【００２０】③従来のＰＬＬ制御は．分周比の変更が行われた場合、そのときの状態から帰還制御を開始するために．分周比の変更が大きく行われた場合は、ロックアップ時間が長くかかる。本発明の制御回路（１３）は，図３に示す如く．キー操作等にて分周比の設定変更が行われた場合（Ｓ１のＹ）．記憶手段（１４）より分周比とアップダウンカウンタ（９）の出力値との相関関係を読み出す（Ｓ２）。相関関係はそれぞれの分周比に対応したアップダウンカウンタ（９）出力値の表形式でもよく．最小二乗法等の統計学による関数でもよい。この相関関係により．分周比の変化値に対応するアップダウンカウンタ（９）の変化値を計算し、この値をアップダウンカウンタ（９）へ出力する（Ｓ３）。この値を初期値として、ＰＬＬの帰還動作を行う（Ｓ４）。

【００２１】更に、位相比較器（５）からのロックアップ信号により（Ｓ５のＹ）．このときのアップダウンカウンタ（９）の出力値でもって、記憶手段（１４）の前記相関関係のデータを更新（学習）する（Ｓ６）。

【００２２】従来は、ループによる動作をしないと減衰の収束値が分からなかった。しかし．本発明はアップダウンカウンタ（９）やラッチ（１０）がデジタル信号であるために容易に想定する電圧をチャージポンプ（６）から出力することができる。このために、ロックアップ時間を短縮することができ．特に、分周比の変更が大きく行われた場合の効果は絶大である。

【００２３】④クロックパルス（８）とラッチ（１０）は出力がデジタルであるため、制御回路（１３）はこの出力値を記憶手段（１４）に記憶させ．記憶させた出力値を次の回路に入力することが容易である。そして、電圧制御発振器（１）とチャージポンプ（６）間を遮断しても．低域濾波器（１２）の制御電圧を保持することができる。

【００２４】例えば．図４に示す如く．制御回路（１３）は、位相比較器（５）からのロック信号を受信すると（Ｓ７）．ラッチ（１０）の出力値を記憶手段（１４）に記憶させ（Ｓ８）．この出力値を記憶手段（１４）より読み出してデジタルアナログコンバータ（１１）に出力する（Ｓ９）。そして．ラッチ（１０）とデジタルアナログコンバータ（１１）の間を遮断し（Ｓ１０）．位相比較器（５）とチャージポンプ（６）の間を遮断する（Ｓ１１）。次に．プログラマブル分周器（２）への電源の供給（図示せず）を遮断してこれを不動作にする（Ｓ１２）。

【００２５】このようにして、ループが遮断され．プログラマブル分周器（２）が不動作となるが、記憶されているラッチ（１０）の出力値により低域濾波器（１２）の制御電圧を保持することができる。そして、ループが遮断されることにより、位相比較器（５）の変化によるノイズがなくなり、また．ノイズが生じてもノイズがループすることはなく、ノイズに強いＰＬＬシンセサイザを供給することができる。更に、プログラマブル分周器（２）を不動作にすることにより、消費電力を少なくすることができる。

【００２６】上述の例では特に消費電力大きいプログラマブル分周器（２）のみを不動作にしたが、分周器（４）や位相比較器（５）やアップダウンカウンタ（９）を不動作にしても低域濾波器の出力制御電圧を保持することができる。

【００２７】また、上述の例ではラッチ（１０）の出力値に基づきＤＡＣ（１１）を制御したが、アップダウンカウンタ（９）の出力値に基づきラッチ（１０）を制御（９）してもよい。

【００２８】⑤基準周波数発振器から出力される周波数は温度により僅か変化する。このために制御回路（１３）は、予め記憶手段（１４）に所定の分周比におけるアップダウンカウンタの出力値と基準周波数発振器の温度の相関関係を記憶させておく。そして、記憶手段（１４）より読み出した相関関係を用いて．設定されている分周比とアップダウンカウンタの出力値より基準周波数発振器を温度補正する。これにより．精度の高い温度制御が可能となる。

【００２９】

【発明の効果】チャージポンプ（６）内部での処理がデジタル信号であるために．マイクロコンピュータやＲＡＭや論理素子等を使用したデジタル制御が容易である。この記憶や制御により、省電力や温度補正を行うことができる。また．ノイズに強いＰＬＬシンセサイザーを供給することができる。

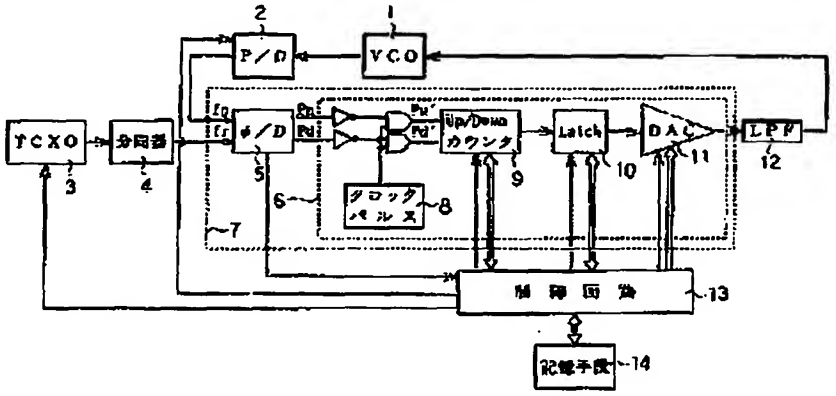
【００３０】更に、ロックアップ時間を短縮するために．チャージポンプを２つ設けてこれを切り替えたり，抵抗を２つ設けてこれを切り替えたりする対策を必要としない。

【図面の簡単な説明】

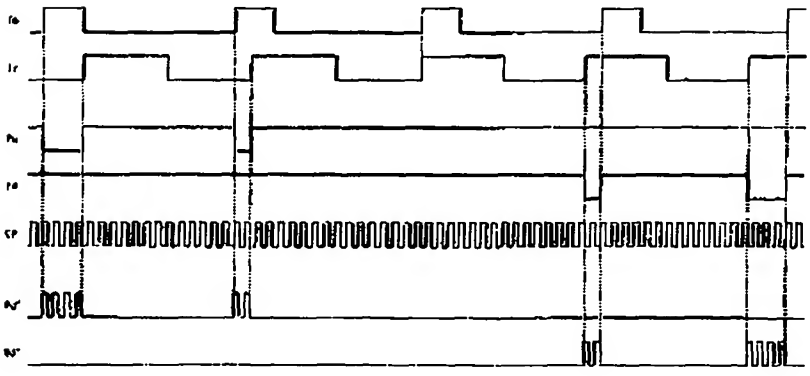
7　　8

【図１】本発明の実施例を示すブロック図である。
【図２】実施例のタイミングチャートである。
【図３】実施例の制御回路のロックアップタイムが早い動作を示す図である。
【図４】実施例の制御回路のノイズに強く且つ省電力となる動作を示す図である。
【図５】従来のチャージポンプを有するＰＬＬシンセサイザーの構成を示すブロック図である。
【図６】従来のチャージポンプの構成を示す図である。
【図７】従来のタイミングチャートである。
【図８】従来のロックアップタイムを早める対策を施したブロック図である。
【符号の説明】
１　電圧制御発振器
＊２　プログラマブル分周器
３　温度補償水晶発振器
４　分周器
５　位相比較器
６　チャージポンプ
７　位相比較器
８　クロックパルス
９　アップダウンカウンタ
１０　ラッチ
１１　デジタルシグナルコンバータ
１２　低域濾波器
１３　制御回路
１４　記憶手段

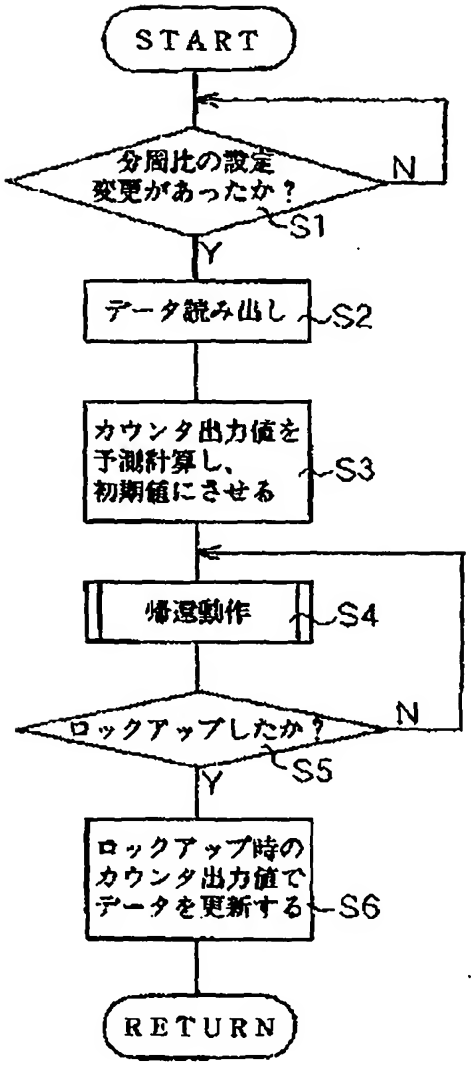
【図１】



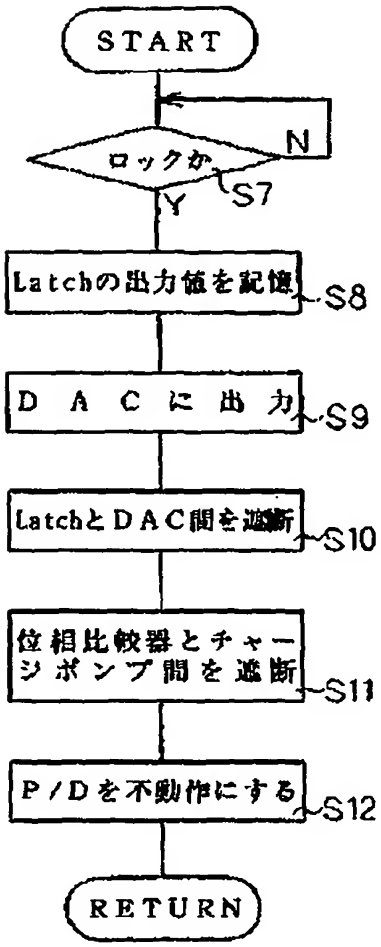
【図２】



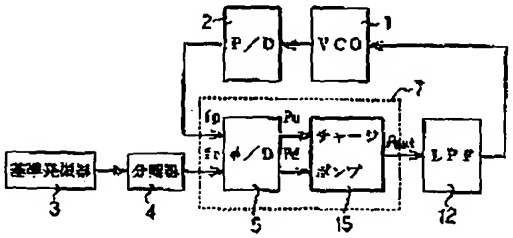
【図3】


START
分周比の設定
変更があったか？
N
S1
Y
データ読み出し
S2
カウンタ出力値を
予測計算し、
初期値にさせる
S3
帰還動作
S4
ロックアップしたか？
N
S5
Y
ロックアップ時の
カウンタ出力値で
データを更新する
S6
RETURN

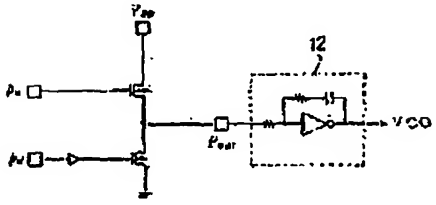
【図4】


START
ロックか
N
S7
Y
Latchの出力値を記憶
S8
D A C に 出 力
S9
LatchとDAC間を遮断
S10
位相比較器とチャージポンプ間を遮断
S11
P/Dを不動作にする
S12
RETURN

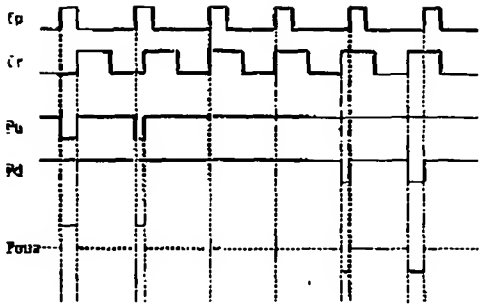
【図5】


2
P/D
VCO
1
7
fp
fv
Pu
Pd
チャージ
ポンプ
LPF
基準発振器
分周器
3
4
5
15
12

【図6】


12
VCO

【図7】



【図8】